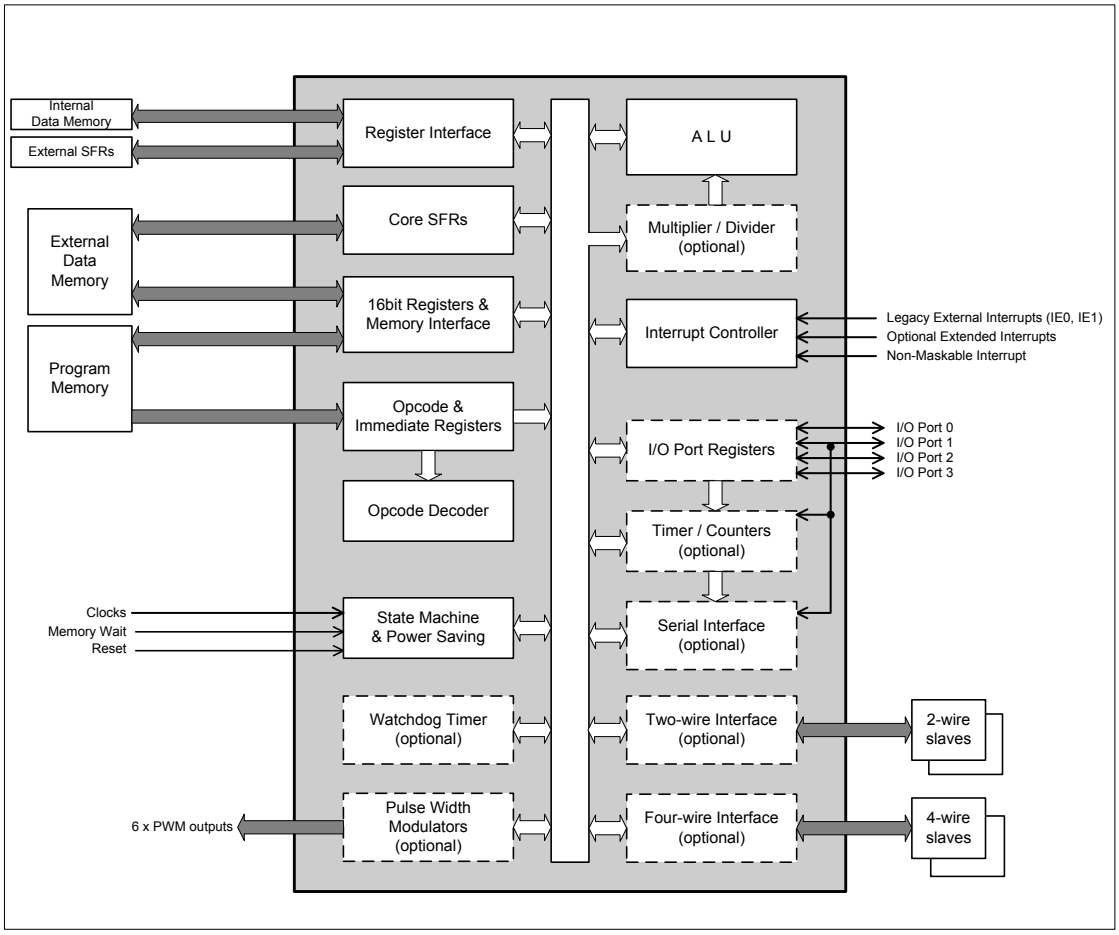
Mentor Graphics M8051W
Fast 8-bit Microcontroller

Overview

The M8051W is a highly configurable soft-core implementation of the industry standard 8051 microcontroller that features a two-clocks-per-machine cycle architecture. Use of standard synchronous design methodology makes this core simple to integrate into both ASIC and FPGA SoC designs.

M8051W Architecture



- Binary and Memory cycle compatible with Intel 8051 Designs
- Fast 2-clocks per machine cycle implementation
- 1Mbyte program and data address spaces
- Memory interfaces may be configured for synchronous or asynchronous devices
- External interfaces support wait states
- Optional demultiplexed program and data interfaces
- Optional single machine cycle memory accesses
- Up to eight 16-bit data pointers
- 25-input, five level interrupt controller
- Full implementation of legacy peripherals: 32 GPIO ports, three 16-bit counter timers and a full-duplex serial port. All legacy peripherals are optional
- Watchdog timer
- Two-wire and Four-wire interfaces
- Pulse width modulator array
- Flexible interfacing options for external peripherals
- Power saving modes: powerdown, stasis, idle and run

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Configurable

The core RTL is highly configurable at compile time allowing users to implement only the features required by their application.

Major configuration options include:

- Combined program and data address space or Harvard architecture
- Optional 20-bit (1Mbyte) extended memory addressing scheme with additional stack
- Number of 16-bit data pointers (1, 2, 4 or 8)
- Each memory component may use a synchronous or asynchronous interface
- Hardware multiplier/divider is optional
- The number of interrupt sources (up to 25) and priority levels (up to 5)
- All peripherals are optional and may be excluded if not required
- Debug traceback depth and number of hardware triggers selectable

Configurable Peripherals

The core includes the following peripherals as standard.

- Three timer/counters
- Legacy UART
- Watchdog timer
- Two-wire interface
- Four-wire interface
- Pulse width modulators, with ramping option

All the non-legacy peripherals include a configurable clock prescaler, and have configurable base addresses and interrupt channels.

Power Management

The M8051W offers three power saving states. These are implemented by dividing the core logic into several synchronous clock domains using optional clock gates. These reduce power consumption by 75% in the idle state and to leakage levels in the stasis and powerdown states. The microcontroller can be awoken from idle and stasis states using interrupts.

Programming Support

The core runs all standard 8051 binary code. Syntill8 recommends Keil C51 and IAR Systems compilers for code development. These compilers can optimise code by making use of the M8051W data pointer and interrupt extensions.

Deliverables

- VHDL '93 and Verilog 2001 RTL source code
- RTL configuration script
- VHDL and Verilog Testbenches
- Demonstration assembly code
- Simulation scripts for Modelsim and Cadence
- Synopsys synthesis compile scripts and SDC timing constraint files
- Example Mentor DFT and ATPG scripts
- Example netlist implementation with SDF files
- Detailed product specification and a user guide containing implementation notes.

M8051 Product Selector

Design	Clocks per Machine Cycle	External Address Space	Internal Data Memory	Multiplexed External Memory Bus	Wait States Support	Synchronous Memory Support	Interrupt Sources	Non-maskable Interrupt	Interrupt Levels	Data Pointers	I/O ports	Timer Counters	Serial Port	Memory Banking	External SFR Interface	On-chip Debug
M8051	12	0-64K	0-256	✔			5		2	1	32	2	1	✔	✔	
M8052	12	0-64K	0-256	✔			6		2	1	32	3	1	✔	✔	
M8051W	2	0-1M	0-256	✔	✔	✔	05-25	✔	3/5	1/2/4/8	0/32	0/2/3	0/1	✔	✔	
M8051EW	2	0-1M	0-256	✔	✔	✔	05-25	✔	3/5	1/2/4/8	0/32	0/2/3	0/1	✔	✔	✔